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1 **A sub-40-ns chain FRAM architecture with 7-ns cell-plate-line drive**
Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999
Pages:1557 - 1563

[Abstract] [PDF Full-Text (340 KB)] **IEEE JNL**

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